

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Michael B. Ball

Patent No.: 6,784,023 B2

Issued: August 31, 2004

For: METHOD OF FABRICATION OF STACKED SEMICONDUCTOR DEVICES

Attorney Docket No.: 2269-2769.6US

CERTIFICATE OF MAILING

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Leta M. Howard

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Attn.: Certificate of Corrections Branch

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Sir:

It is noted that several errors appear in this patent of a typographical nature. These errors are due to mistakes in printing on the part of the U.S. Patent and Trademark Office, and occurred through no fault of the Applicant. A certificate of correction in the form attached hereto is requested. Certificate

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Correction

Please send the Certificate to:

Name:

James R. Duzan

Address:

TraskBritt

P.O. Box 2550

Salt Lake City, Utah 84110

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Attached hereto in duplicate is Form PTO/SB/44 with at least one copy being suitable for printing.

Respectfully submitted,

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Date: March 23, 2007

JRD/csw

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Enclosures: PTO/SB/44 in duplicate

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UNITED STATES PATENT AND TRADEMARK OFFICE

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Page 1 of 1

DATED

August 31, 2004

INVENTOR(S):

Michael B. Ball

It is certified that errors appear in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

On the title page:

In ITEM (56) "References Cited"

after the last entry appearing in the "FOREIGN PATENT

DOCUMENTS" section, insert:

-- OTHER PUBLICATIONS

IBM Technical Disclosure Bulletin, P.F. Iafrate, High Density and Speed Performance Chip Joining Procedure and Package, Vol. 15, No. 4, Pg. 1281.--

In the specification:

COLUMN 1, LINE 7,

change "pending," to --now U.S. Patent 6,337,227 issued

Jan. 8, 2002,--

MAILING ADDRESS OF SENDER:

PATENT NO. <u>6,784,023 B2</u>

James R. Duzan 230 South 500 East, Suite 300 Salt Lake City, Utah 84102 USA

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